

FIG. 1

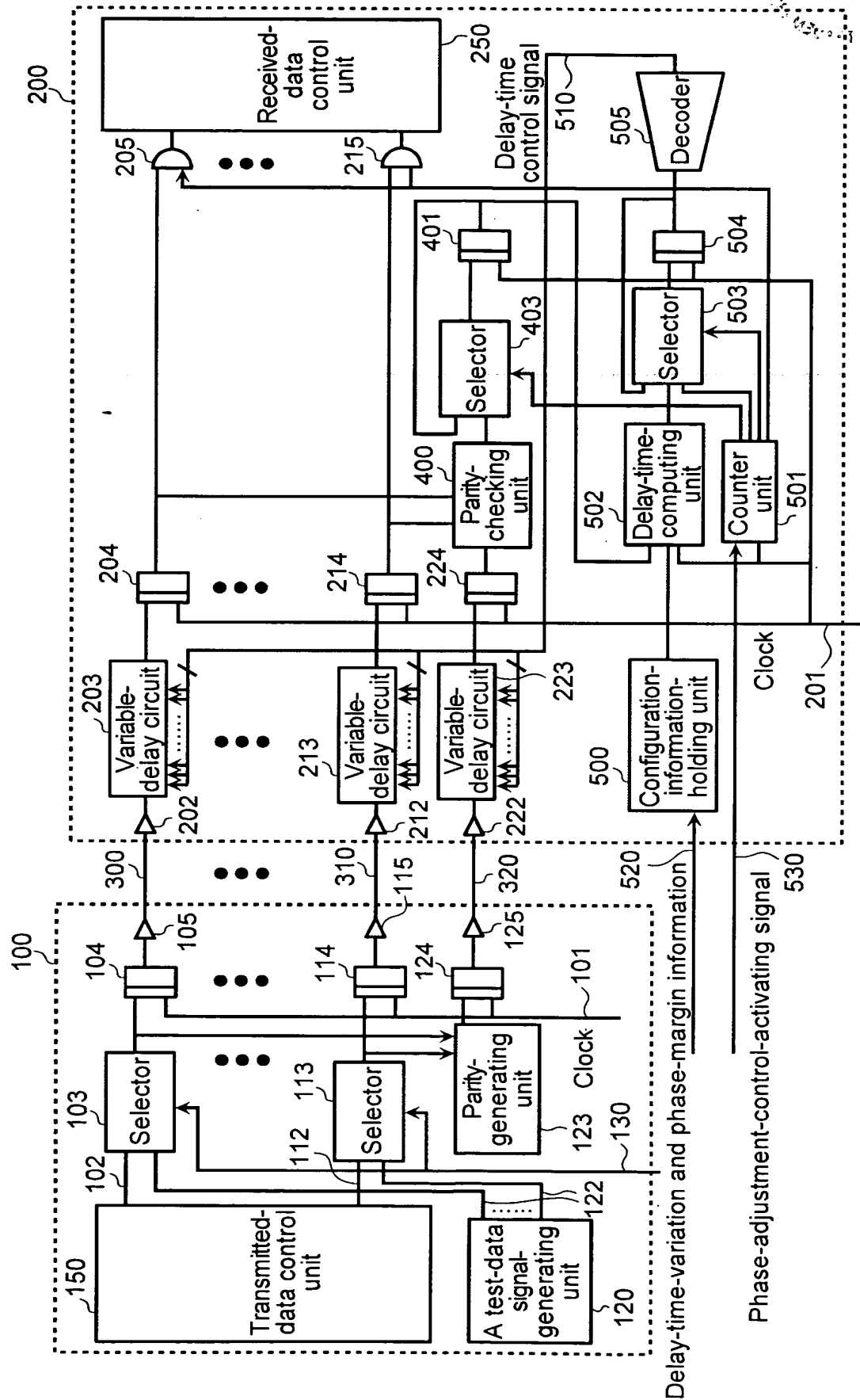


FIG.2

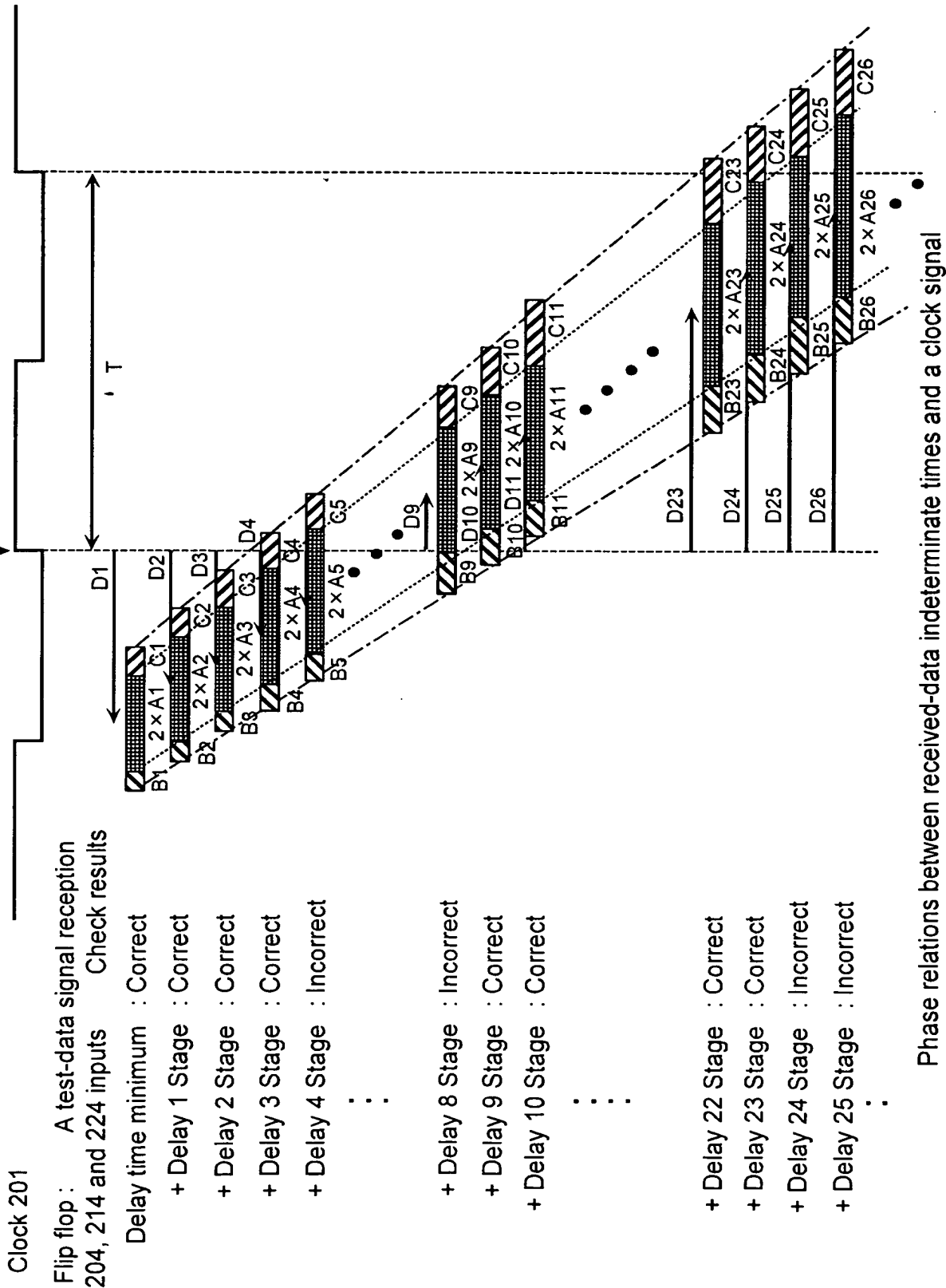


FIG.3

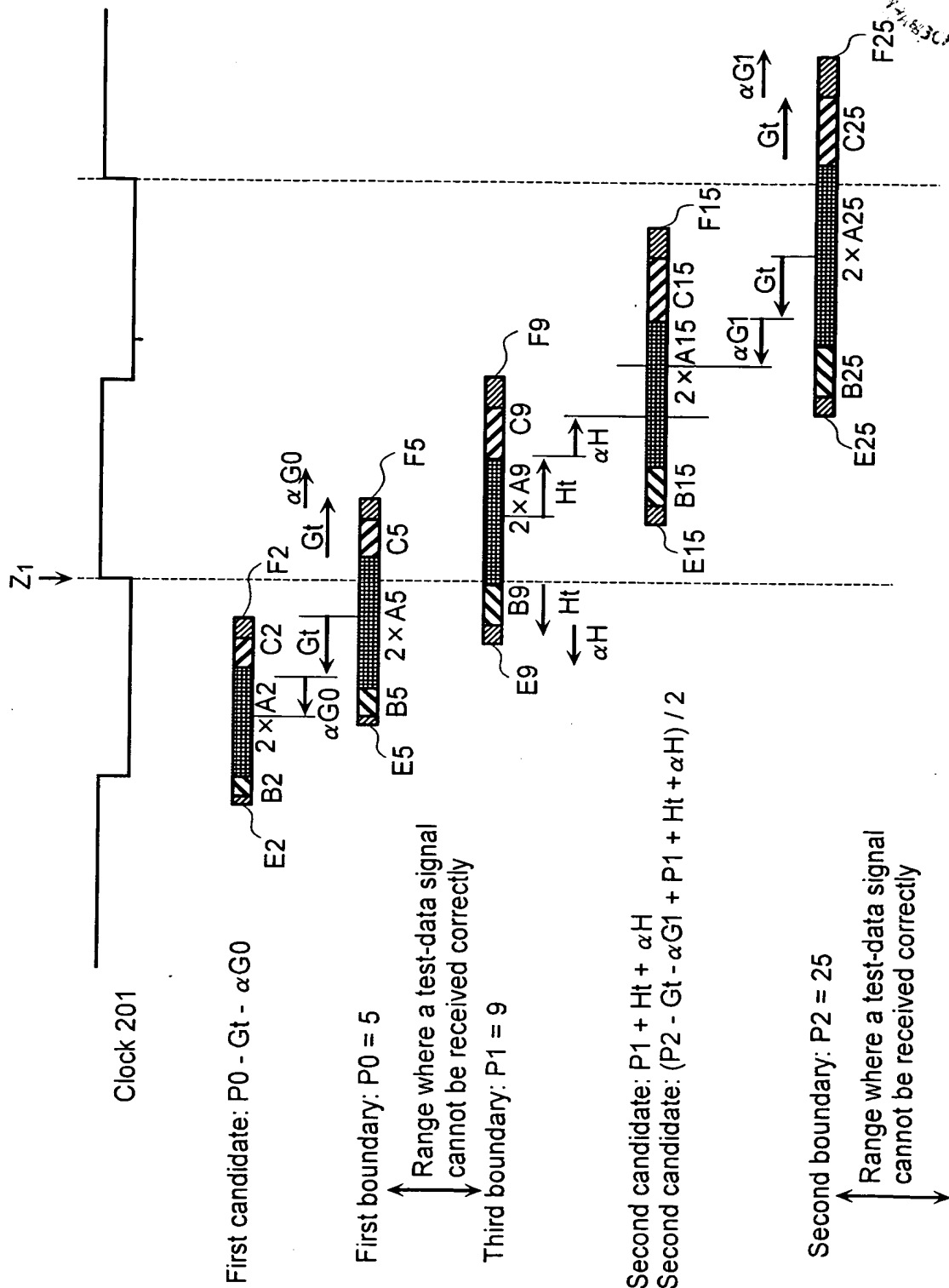
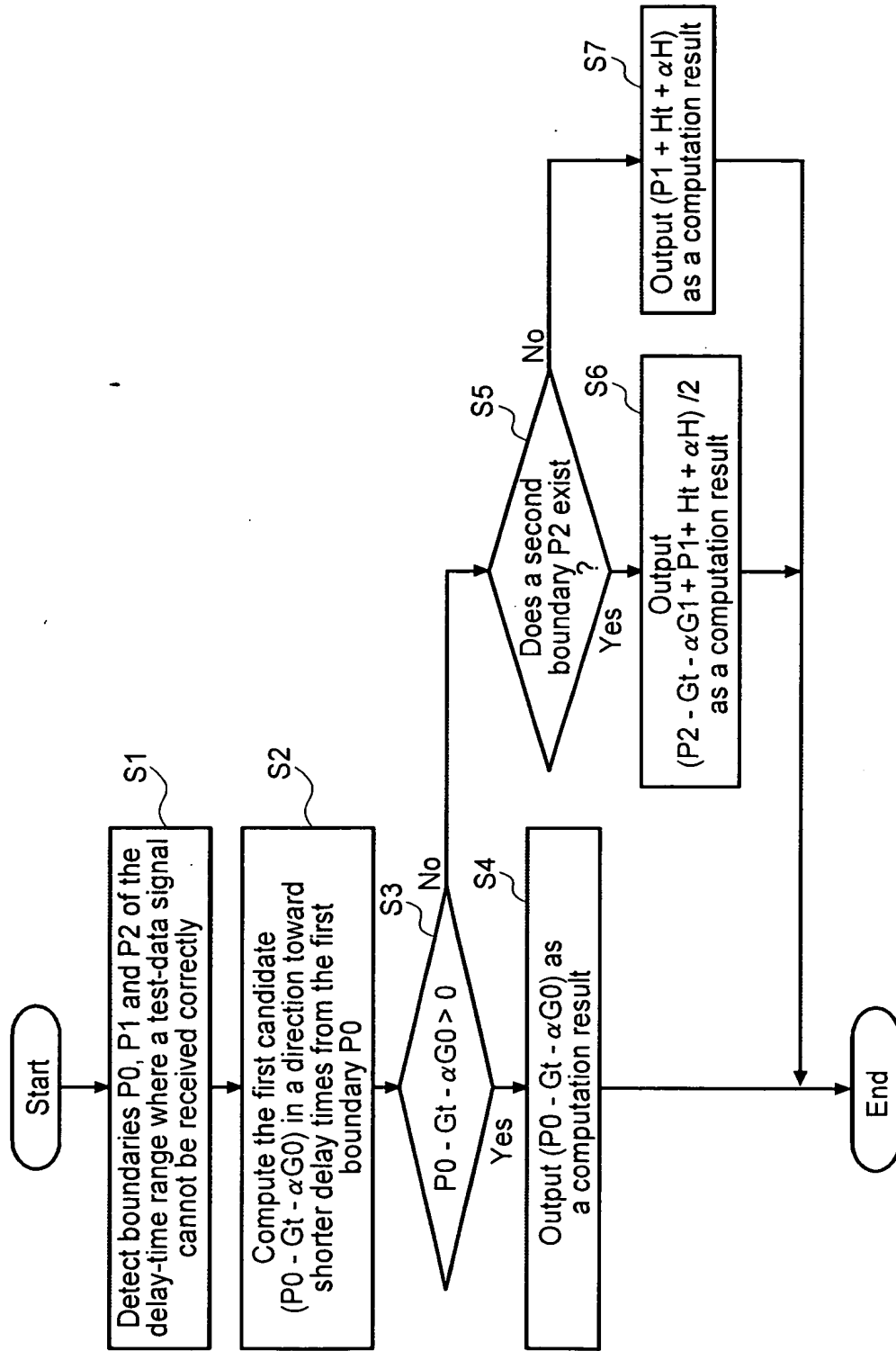
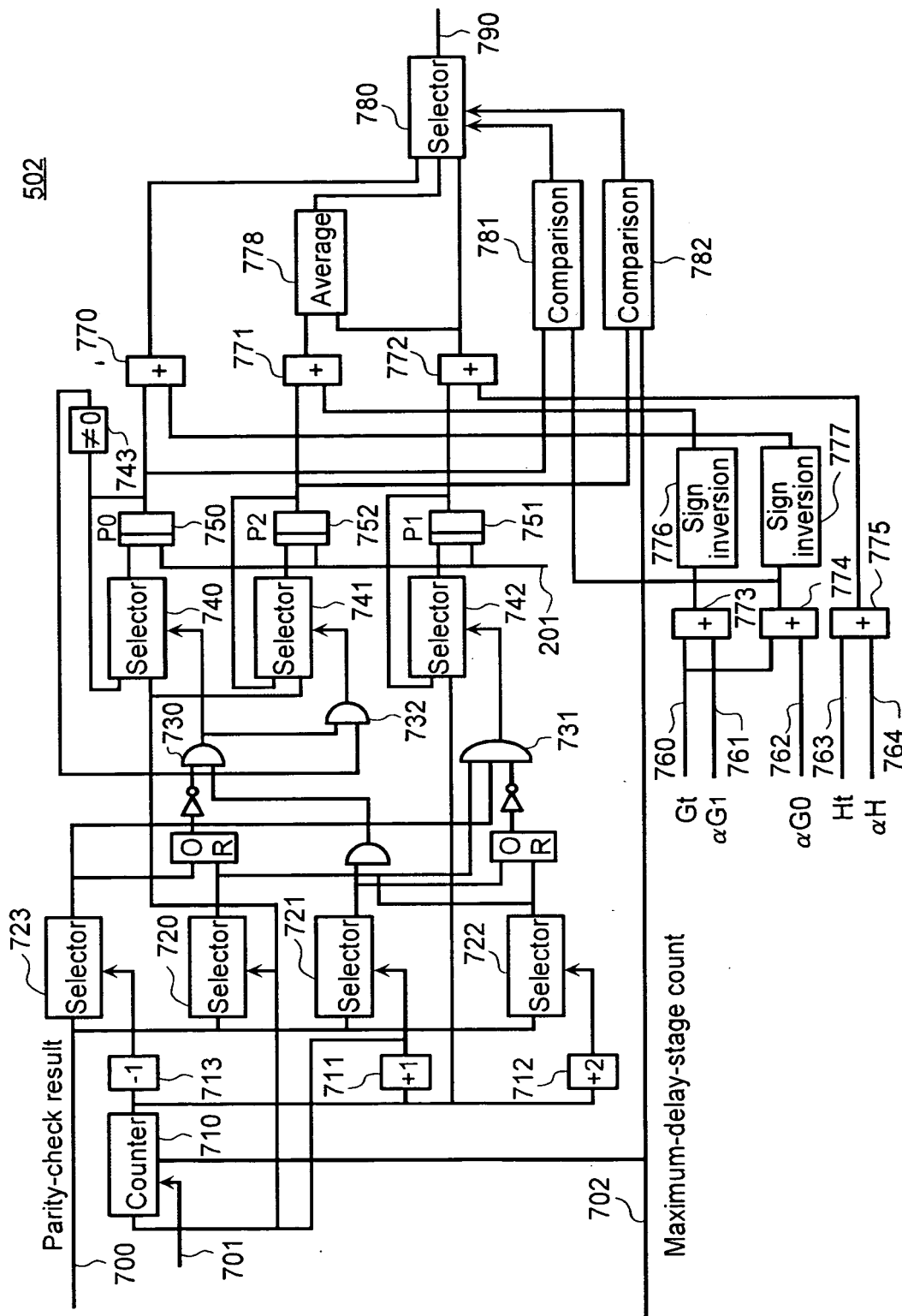


FIG.4



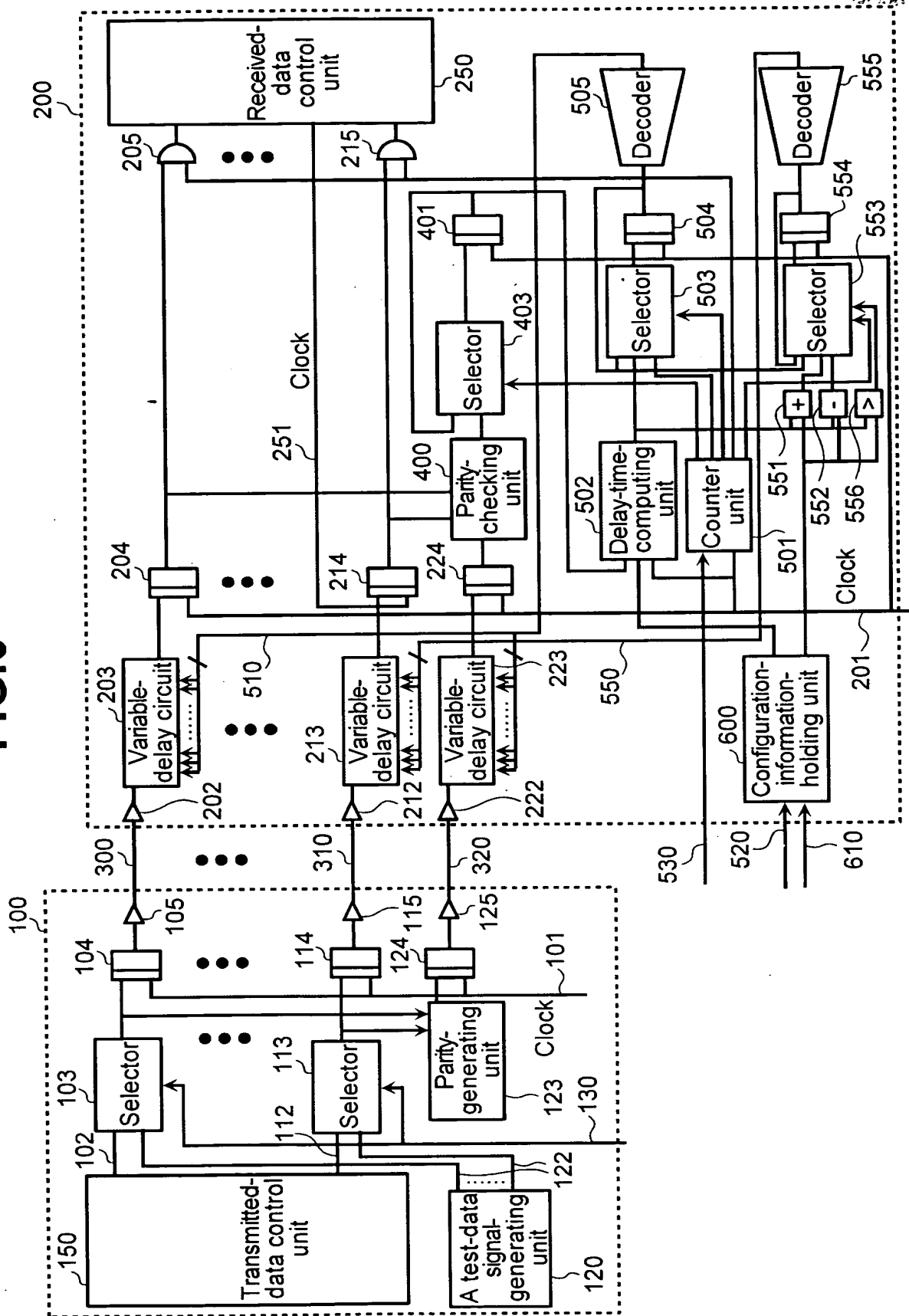
Algorithm of the delay-time computation

FIG. 5



Typical circuit configuration of delay-time-computing unit

FIG.6



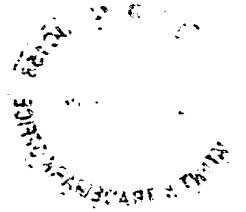


FIG.7

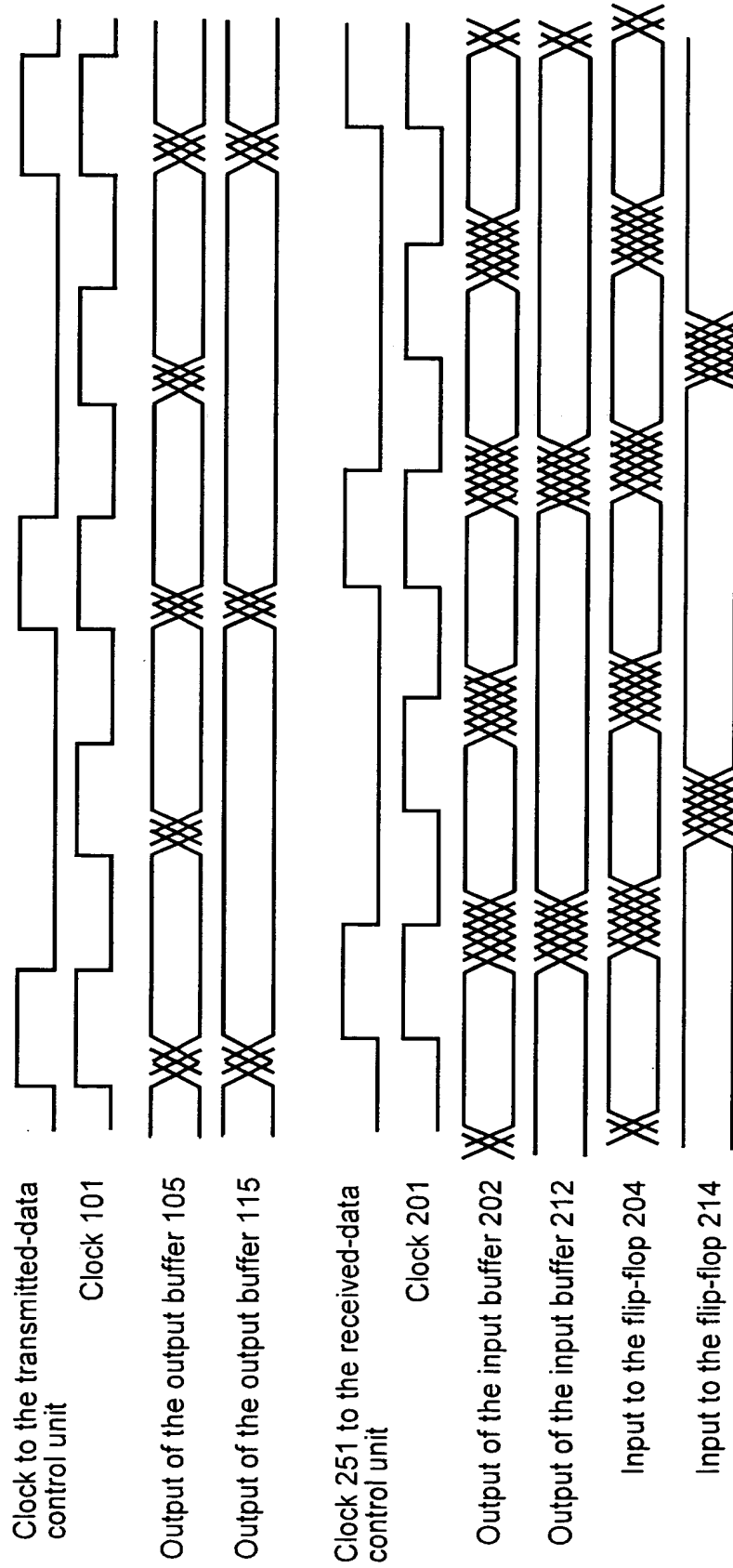


FIG. 8.

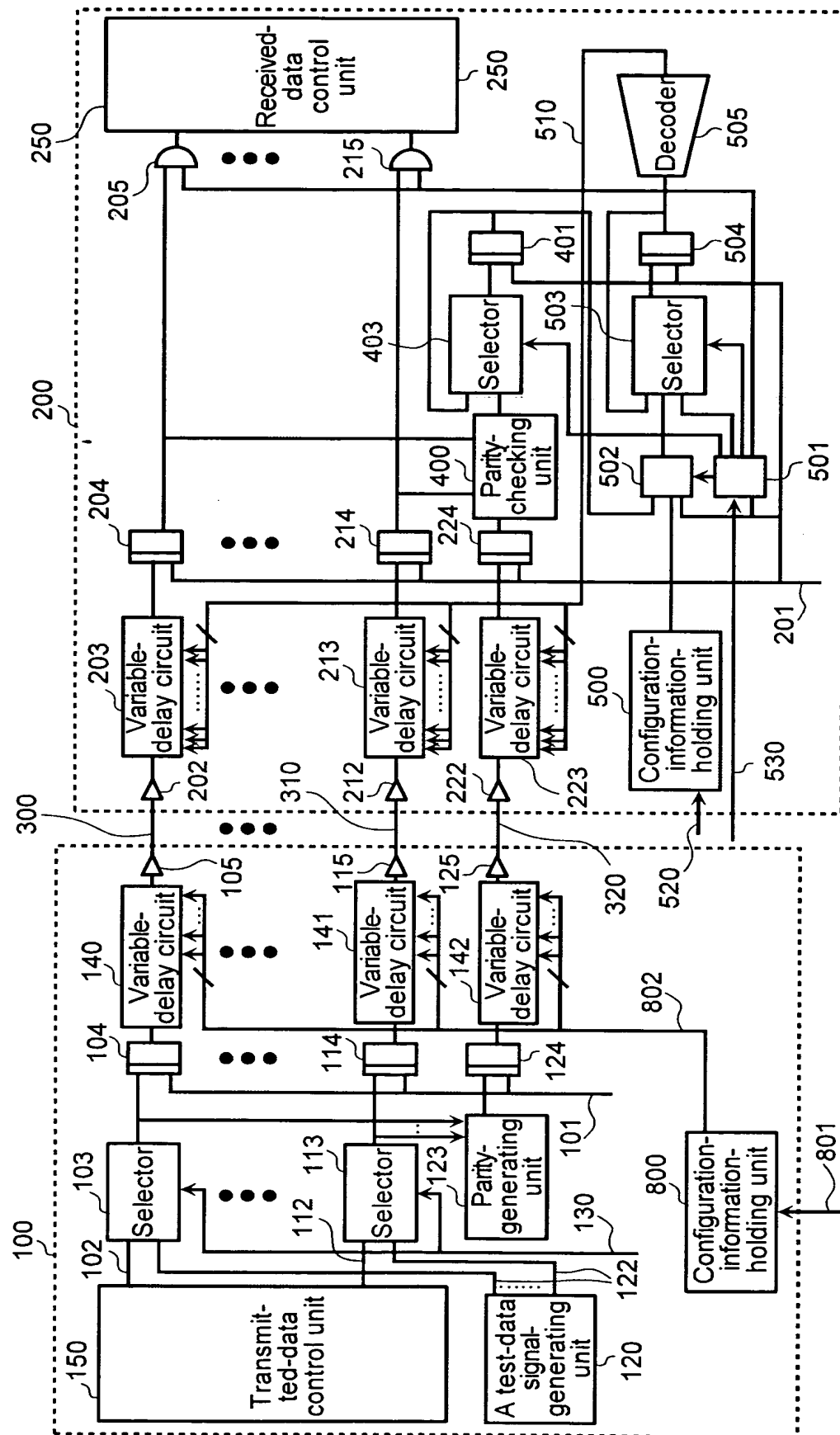
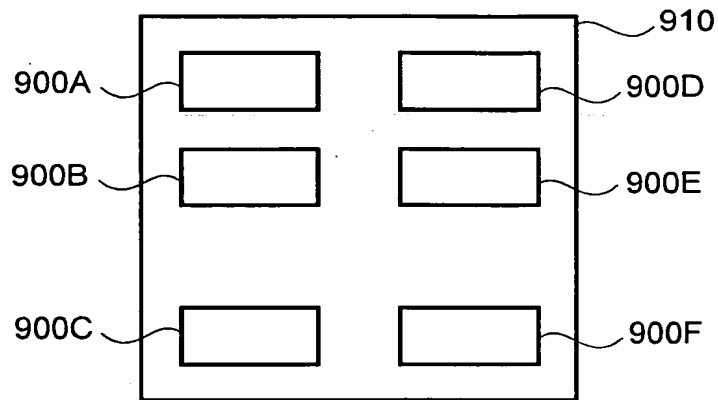


FIG.9

Single Circuit



Multi-Circuit
Chip



Multi-Chip
Device

